WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:

a SOI wafer having a stacked structure of a first silicon layer, a buried insulating film and a second silicon layer;

a trench formed by removing a predetermined region of the second silicon layer;

a first silicide layer formed at side walls of the trench;

a device isolation film defining an active region of the SOI wafer formed by filling the trench;

a gate electrode having a gate insulation film formed on the active region of the SOI wafer;

an insulation spacer formed at side walls of the gate electrode;

impurity junction regions formed at both sides of the gate electrode in the active region of the SOI wafer; and

a second silicide layer formed on the gate electrode and the impurity regions.

2. The semiconductor device according to claim 1, wherein the first and the second silicide layers comprise a metal selected from the group consisting of titanium, cobalt, nickel, and tungsten.

3. A method of forming a semiconductor device, comprising the steps of:

forming a pad insulating film on a SOI wafer having a stacked structure of a first silicon layer, a buried insulating film and a second silicon layer;

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

etching a predetermined region of the pad insulating film and the second silicon layer by a lithography process using a device isolation mask to form a trench exposing the buried insulating film;

forming a first silicide layer at side walls of the trench;

forming a device isolation film defining an active region by filling the trench;

forming a transistor having a gate electrode, an insulation spacer, and impurity junction regions on the second silicon layer in the active region; and

forming a second silicide layer on the gate electrode and the impurity junction regions.

4. The method according to claim 3, wherein the step of forming the first silicide layer comprises the steps of forming a high melting point metal layer on the entire surface having a thickness in a range of 100 – 300Å using a CVD method, performing an annealing process, and removing an unreacted portion of the high melting point metal layer.

5. The method according to claim 4, wherein the high melting point metal layer comprises a metal selected from the group consisting of titanium, cobalt, nickel, and tungsten.

6. The method according to claim 4, wherein the annealing process is performed at the temperature in a range of 900 – 1000 °C for 10 – 60 seconds.

7. The method according to claim 4, wherein the step of removing the unreacted portion of the high melting point metal layer comprises performing a first wet etch process using a HNO_3 solution and a second wet etch process using a HF solution diluted in the HNO_3 solution.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com

8. The method according to claim 3, wherein the step of forming the second silicide layer comprises the steps of forming a high melting point metal layer of a predetermined thickness on the entire surface, performing a first annealing process at a temperature in a range of 650 – 750 °C for 10 – 30 seconds, removing an unreacted portion of high melting point metal layer, and performing a second annealing process at a temperature in a range of 800 – 1000 °C for 10 – 30 seconds.

9. The method according to claim 8, wherein the high melting point metal layer comprises a metal selected from the group consisting of titanium, cobalt, nickel, and tungsten.

FINNEGAN
HENDERSON
FARABOW
GARRETT &
DUNNER LLP

1300 I Street, NW
Washington, DC 20005
202.408.4000
Fax 202.408.4400
www.finnegan.com